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Notice of Allowability	Application No. 10/694,506	Applicant(s) GOTOH ET AL.	
	Examiner Prasad R. Akkapeddi	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *10/27/2003*.

2. ☒ The allowed claim(s) is/are *1-10*.

3. ☒ The drawings filed on *27 October 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 10/27/2003
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-10 are allowed.

2. The following is an examiner's statement of reasons for allowance:

A search of the prior art did not disclose an active matrix substrate or a display device such an active matrix substrate comprising a combination of structural elements, more specifically:

(a) A semiconductor layer formed above a storage capacitor via a first insulating layer;

(b) A first light-shielding layer formed above a semiconductor layer via a second insulating layer to cover at least a channel region of the semiconductor layer and a third insulating layer formed on the first light-shielding layer;

(c) A source electrode layer including a source electrode and a drain electrode formed on the third insulating layer;

(d) A fourth insulating layer formed on the source electrode layer;

(e) A pixel electrode formed on the fourth insulating layer and electrically connected to the drain electrode and

(f) The first light-shielding layer is conductive and has a drain-side light-shielding portion electrically connected to one of a pair of electrodes of the storage capacitor and also electrically connected to the drain electrode.

The uniqueness of the invention is in the placement of the first light-shielding layer and its electrical connection to the storage capacitor.

The prior art by (a) In Fig. 14, Murade (U.S.Patent Application Publication US 2004/0004221), teaches the storage capacitor (70) is along the side and separated from a semiconductor layer (1a) and the light shielding layer (11a) is below the semiconductor layer and not in between the storage capacitor and the semiconductor as recited in the instant claims.

(b) In Fig. 8, Iki et al., (U.S.Patent Application Publication US 2004/0056297), teach that the storage capacitor (70) is above the semiconductor layer (1) and the light-shielding layer (11a) is below the semiconductor layer.

(c) In Fig. 3, Sato (U.S.Patent Application Publication US 2004/0051822) teaches that the storage capacitor (70) is above the semiconductor layer (1) and the light-shielding layer (6a) is above the storage capacitor and the semiconductor layer.

(d) In Fig. 3, Fumiaki et al. (JP 2001-06638), Applicant disclosed prior art, discloses a semiconductor layer (7) above a storage capacitor (3,4). However, the light-shielding layer (19) is above the source and the drain regions of the semiconductor layer and not in between the storage capacitor and the source and drain regions as recited in the instant claims.

Hence, the case is allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R. Akkapeddi whose telephone number is 571-272-2285. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Prasad R Akkapeddi, Ph.D
Examiner
Art Unit 2871

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800